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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 09-064076

(43)Date of publication of application : 07.03.1997

(51)Int.Cl. H01L 21/56

(21)Application number : 07-217482

(22)Date of filing : 25.08.1995

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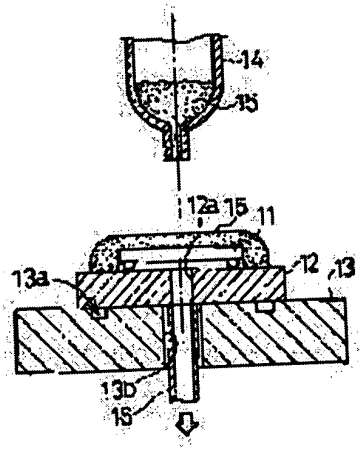
(54) SEALING BOARD OF IC CHIP AND SEALING DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To obtain the sealing board of an IC chip, the method of sealing and a sealing device with high productivity by providing a sealing material sucking hole through which the sealing material applied around the IC chip mounted on a mounting position is sucked and filling the gap between the IC chip and the sealing board with the sucked sealing material.

SOLUTION: A sealing material applying means 14, which moves in the direction of X, Y and Z relatively to a sealing stage 13, applies sealing material 15 around an IC chip 11 mounted on a sealing board 12. The sealing material sucking means 16 sucks the sealing material 15 applied to the IC chip 11 through a sealing material sucking through hole 12a and sealing material sucking hole 13b, and fills the gap between the IC chip 11 and the sealing board 12 with the sucked sealing material 15 by force. Therefore, the productivity is improved drastically compared with the case before of flowing the sealing material into the gap between the IC chip and the board with the help of the inclination of the sealing board for a long time of 10 minutes.



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LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

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[Date of final disposal for application]

[Patent number]

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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The closure substrate of IC chip characterized by establishing the sealing agent attraction hole filled up with the sealing agent with which the sealing agent applied to the periphery of IC chip mounted in said mounting position was attracted, and the above attracted the clearance between said IC chips and said closure substrates in IC chip mounting position of the closure substrate which carries out flip chip mounting of the IC chip.
[Claim 2] The closure substrate of IC chip characterized by establishing the sealing agent impregnation hole which pours into the clearance between said IC chips and said closure substrates the sealing agent which closes IC chip mounted in said mounting position in IC chip mounting position of the closure substrate which carries out flip chip mounting of the IC chip.
[Claim 3] A sealing agent attraction hole is established in IC chip mounting position of the closure substrate which carries out flip chip mounting of the IC chip. Mount IC chip in said mounting position, and a sealing agent is applied to the periphery of said mounted IC chip. The closure approach of IC chip characterized by filling up with the sealing agent with which said applied sealing agent was attracted and the above attracted the clearance between said IC chips and said closure substrates from said sealing agent attraction hole on the background of the closure substrate side which mounted said IC chip.
[Claim 4] The closure approach of the IC chip characterized by to fill up with the sealing agent with which the sealing agent was poured in and the above poured in the clearance between said IC chips and said closure substrates from said sealing agent impregnation hole on the background of the closure substrate side which established the sealing agent impregnation hole in IC chip mounting position of the closure substrate which carries out flip chip mounting of the IC chip, mounted IC chip in said mounting position, and mounted said IC chip.
[Claim 5] The closure stage which has a maintenance means to hold the closure substrate which carries out flip chip mounting of the IC chip, and the sealing agent attraction through hole prepared according to the sealing agent attraction hole in IC chip mounting position of said closure substrate, A sealing agent spreading means to apply a sealing agent to the periphery of IC chip mounted in said closure substrate, The sealing arrangement of IC chip characterized by having a sealing agent attraction means to fill up with the sealing agent with which the sealing agent applied to the periphery of said IC chip through said sealing agent attraction through hole and said sealing agent attraction hole was attracted, and the above attracted the clearance between said IC chips and said closure substrates.
[Claim 6] The sealing arrangement of the IC chip carry out pouring in a sealing agent through the closure stage which has a maintenance means hold the closure substrate which carries out flip chip mounting of the IC chip, and the sealing agent impregnation through hole which prepared according to the sealing agent impregnation hole in IC chip mounting position of said closure substrate, and said sealing agent impregnation through hole and said sealing agent impregnation hole, and having said IC chip and a sealing agent impregnation means are filled up with the sealing agent of the above [the clearance between said closure substrates] which poured in as the description.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the closure approach and substrate of IC chip in a flip chip mounting process.
[0002]
[Description of the Prior Art] In the MCM (multi chip module) mounting process of having used the flip chip mounting process of recently having been brought into the limelight, and flip chip mounting, the approach shown in drawing 5 from the former is common as the closure approach performed after IC chip mounting.
[0003] The conventional example of the closure approach is heated by predetermined temperature, for example, 60-degreeC, in drawing 5 . Adsorption immobilization of the substrate 3 with which the IC chip 2 was mounted to the level surface on the predetermined include angle theta 1, for example, the block leaned 15 degrees, is carried out. A sealing agent (epoxy phenol resin) 5 is applied to upper edge part 2a of the IC chip 2 with a dispenser 4, and by 15-degree dip, a sealing agent 5 flows in between the IC chip 2 and a substrate 3, and closes.
[0004]
[Problem(s) to be Solved by the Invention] However, with the configuration of the above-mentioned conventional example, since it closes by the flow of the sealing agent by dip, closure time amount is long and the trouble that starting productivity is low is in closure of one IC chip for about 10 minutes. In order to make [many] a volume, it is necessary to make [many] the number of stages which does a closure activity, and leads to the trouble that facility cost becomes high.
[0005] This invention solves the above-mentioned trouble and productivity aims [this invention] at offer of the closure substrate of high IC chip, the closure approach, and a sealing arrangement.
[0006]
[Means for Solving the Problem] In order that the closure substrate of IC chip of the 1st invention of this application may solve the above-mentioned technical problem, it carries out having established the sealing agent attraction hole filled up with the sealing agent with which the sealing agent applied to the periphery of IC chip mounted in said mounting position was attracted, and the above attracted the clearance between said IC chips and said closure substrates in IC chip mounting position of the closure substrate which carries out flip chip mounting of the IC chip as the description.
[0007] The closure substrate of IC chip of the 2nd invention of this application is characterized by establishing the sealing agent impregnation hole which pours into the clearance between said IC chips and said closure substrates the sealing agent which closes IC chip mounted in said mounting position in IC chip mounting position of the closure substrate which carries out flip chip mounting of the IC chip, in order to solve the above-mentioned technical problem.
[0008] In order that the closure approach of IC chip the 3rd invention of this application may solve the above-mentioned technical problem A sealing agent attraction hole is established in IC chip mounting position of the closure substrate which carries out flip chip mounting of the IC chip. Mount IC chip in

said mounting position, and a sealing agent is applied to the periphery of said mounted IC chip. It is characterized by filling up with the sealing agent with which said applied sealing agent was attracted and the above attracted the clearance between said IC chips and said closure substrates from said sealing agent attraction hole on the background of the closure substrate side which mounted said IC chip.
[0009] In order that the closure approach of the IC chip the 4th invention of this application may solve the above-mentioned technical problem, it carries out pouring in a sealing agent from said sealing agent impregnation hole on the background of the closure substrate side which established the sealing agent impregnation hole in IC chip mounting position of the closure substrate which carries out flip chip mounting of the IC chip, mounted IC chip in said mounting position, and mounted said IC chip, and being filled up with the sealing agent of the above [the clearance between said IC chips and said closure substrates] poured in as the description.
[0010] In order that the sealing arrangement of IC chip of the 5th invention of this application may solve the above-mentioned technical problem The closure stage which has a maintenance means to hold the closure substrate which carries out flip chip mounting of the IC chip, and the sealing agent attraction through hole prepared according to the sealing agent attraction hole in IC chip mounting position of said closure substrate, A sealing agent spreading means to apply a sealing agent to the periphery of IC chip mounted in said closure substrate, It is characterized by having a sealing agent attraction means to fill up with the sealing agent with which the sealing agent applied to the periphery of said IC chip through said sealing agent attraction through hole and said sealing agent attraction hole was attracted, and the above attracted the clearance between said IC chips and said closure substrates.
[0011] In order that the sealing arrangement of IC chip of the 6th invention of this application may solve the above-mentioned technical problem The closure stage which has a maintenance means to hold the closure substrate which carries out flip chip mounting of the IC chip, and the sealing agent impregnation through hole prepared according to the sealing agent impregnation hole in IC chip mounting position of said closure substrate, It is characterized by having a sealing agent impregnation means to fill up with the sealing agent with which the sealing agent was poured in through said sealing agent impregnation through hole and said sealing agent impregnation hole, and the above poured in the clearance between said IC chips and said closure substrates.
[0012]
[Function] The closure substrate of IC chip of the 1st invention of this application, the closure approach of IC chip the 3rd invention of this application, and the sealing arrangement of IC chip of the 5th invention of this application It has a sealing agent attraction hole in the location where a closure substrate should carry out flip chip mounting of the IC chip. A closure stage has a maintenance means to hold said closure substrate, and the sealing agent attraction through hole prepared according to the sealing agent attraction hole in IC chip mounting position of said closure substrate. A sealing agent spreading means applies a sealing agent to the periphery of IC chip mounted in said closure substrate. Since a sealing agent attraction means fills up with the sealing agent with which the sealing agent applied to the periphery of said IC chip through said sealing agent attraction through hole and said sealing agent attraction hole was attracted, and the above attracted the clearance between said IC chips and said closure substrates compulsorily In the conventional example, the dip of a closure substrate is used and productivity improves substantially as compared with slushing a sealing agent into the clearance between IC chip and a closure substrate over the long time amount for about 10 minutes.
[0013] The closure substrate of IC chip of the 2nd invention of this application, the closure approach of IC chip the 4th invention of this application, and the sealing arrangement of IC chip of the 6th invention of this application It has a sealing agent impregnation hole in the location where a closure substrate should carry out flip chip mounting of the IC chip. A closure stage has a maintenance means to hold said closure substrate, and the sealing agent impregnation through hole prepared according to the sealing agent impregnation hole in IC chip mounting position of said closure substrate. Since a sealing agent impregnation means pours in a sealing agent through said sealing agent impregnation through hole and said sealing agent impregnation hole and fills up compulsorily the clearance between said IC chips and said closure substrates with said sealing agent In the conventional example, the dip of a closure substrate

is used and productivity improves substantially as compared with slushing a sealing agent into the clearance between IC chip and a substrate over the long time amount for about 10 minutes.

[0014]

[Example] The 1st example of the sealing arrangement of IC chip which uses the closure substrate of IC chip of this invention and the closure approach of IC chip is explained based on drawing 1 and drawing 2 .

[0015] In drawing 1 and drawing 2 , flip chip mounting of the IC chip 11 is carried out at the closure substrate 12. It has sealing agent attraction hole 12a in the location where the closure substrate 12 should carry out flip chip mounting of the IC chip 11. It has adsorption slot 13a to which the closure stage 13 adsorbs and holds the substrate which should carry out flip chip mounting of the IC chip, and sealing agent attraction through hole 13b prepared according to sealing agent attraction hole 12a in IC chip mounting position of the closure substrate 12. The sealing agent spreading means 14 which can be displaced relatively in the XYZ direction to the closure stage 13 A sealing agent 15 is applied to the periphery of the IC chip 11 mounted in the closure substrate 12. Since the sealing agent attraction means 16 fills up with the sealing agent 15 with which the sealing agent 15 applied to the IC chip 11 through said sealing agent attraction through hole 12a and said sealing agent attraction hole 13b was attracted, and the above attracted the clearance between said IC chips 11 and said closure substrates 12 compulsorily, in the conventional example The dip of a closure substrate is used and productivity improves substantially as compared with slushing a sealing agent into the clearance between IC chip and a substrate over the long time amount for about 10 minutes.

[0016] In this case, as mentioned above, although the sealing agent 15 is applied to the IC chip 11 whole in drawing 2 , if a sealing agent 15 is applied the periphery of the IC chip 11, i.e., each side of the IC chip 11, the clearance between said IC chips 11 and said closure substrates 12 can be compulsorily filled up with a sealing agent 15 by attraction of the sealing agent attraction means 16.

[0017] Moreover, although one IC chip is mounted and enclosed with the closure substrate 12 in this example, it does not restrict to one piece but, of course, also in two or more cases, is.

[0018] The 2nd example of the sealing arrangement of IC chip which uses the closure substrate of IC chip of this invention and the closure approach of IC chip is explained based on drawing 3 and drawing 4 .

[0019] In drawing 3 and drawing 4 , flip chip mounting of the IC chip 21 is carried out at the closure substrate 22. And adsorption maintenance of the IC chip 21 is carried out by IC adsorption tool 26. It has sealing agent impregnation hole 22a in the location where the closure substrate 22 should carry out flip chip mounting of the IC chip 21. It has sealing agent impregnation through hole 23b prepared according to adsorption slot 23a to which the closure stage 23 adsorbs and holds the closure substrate 22 which should carry out flip chip mounting of the IC chip 21, and sealing agent impregnation hole 22a in IC chip mounting position of said closure substrate 22. The sealing agent impregnation means 24 Since it fills up with the sealing agent 25 with which the sealing agent 25 was poured in through said sealing agent impregnation through hole 23b and said sealing agent impregnation hole 22a, and the above poured in the clearance between said IC chips 21 and said closure substrates 22 compulsorily In the conventional example, the dip of a closure substrate is used and productivity improves substantially as compared with slushing a sealing agent into the clearance between IC chip and a closure substrate over the long time amount for about 10 minutes.

[0020] In this case, if viscosity by temperature management of enclosure material is adjusted proper, it is possible to close [be / it / under / flip chip mounting / concurrency].

[0021] Moreover, if up Shimonoseki charge of IC adsorption tool 26 of drawing 4 and the sealing agent impregnation means 24 is made into reverse, gravity will act on a direction of grouting and impregnation will become easy.

[0022]

[Effect of the Invention] The closure substrate of IC chip of the 1st invention of this application, the closure approach of IC chip the 3rd invention of this application, and the sealing arrangement of IC chip of the 5th invention of this application Since it fills up with the sealing agent with which the sealing

agent attraction means attracted the sealing agent applied to the periphery of IC chip, and attracted the clearance between IC chip and a closure substrate compulsorily, in the conventional example The dip of a closure substrate is used and the effectiveness that productivity improves substantially is done so as compared with slushing a sealing agent into the clearance between IC chip and a closure substrate over the long time amount for about 10 minutes.
[0023] The closure substrate of IC chip of the 2nd invention of this application, the closure approach of IC chip the 4th invention of this application, and the sealing arrangement of IC chip of the 6th invention of this application Since a sealing agent impregnation means fills up with the sealing agent which poured in the sealing agent and poured in the clearance between IC chip and a closure substrate compulsorily, in the conventional example The dip of a closure substrate is used and the effectiveness that productivity improves substantially is done so as compared with slushing a sealing agent into the clearance between IC chip and a closure substrate over the long time amount for about 10 minutes.

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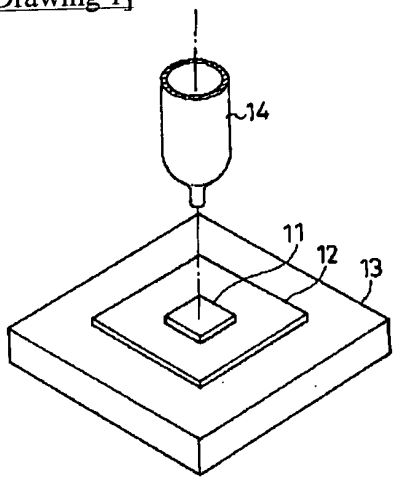
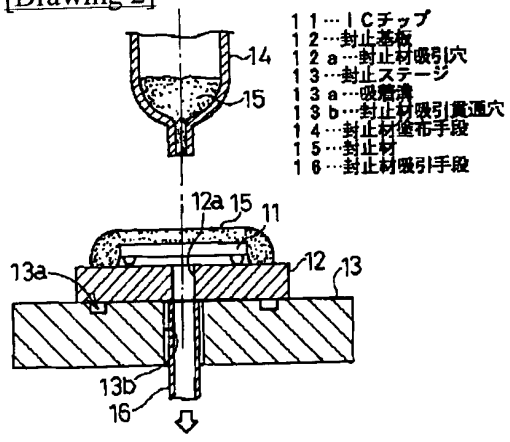
DRAWINGS

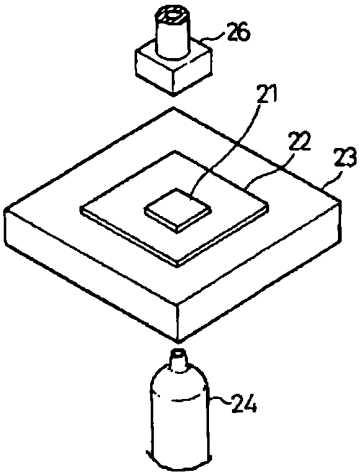
[Drawing 1]



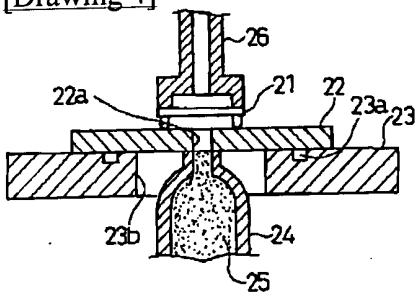
[Drawing 2]



[Drawing 3]

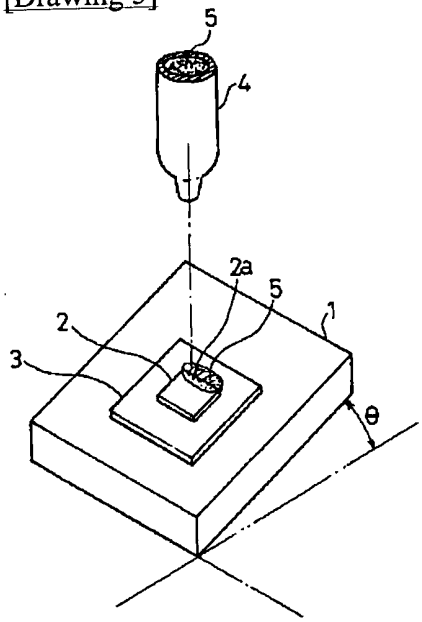


[Drawing 4]



２１…ＩＣチップ
２２…封止基板
２２ａ…封止材注入穴
２３…封止ステージ
２３ａ…吸着溝
２３ｂ…封止材注入貫通穴
２４…封止材注入手段
２５…封止材
２６…ＩＣ吸着ツール

[Drawing 5]



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EP 24959 (2) **EUROPEAN PATENT OFFICE**

Patent Abstracts of Japan

PUBLICATION NUMBER : 09064076
PUBLICATION DATE : 07-03-97

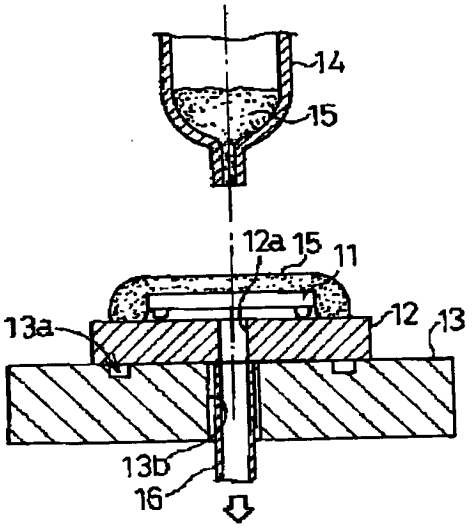
APPLICATION DATE : 25-08-95
APPLICATION NUMBER : 07217482

APPLICANT : MATSUSHITA ELECTRIC IND CO LTD;

INVENTOR : ENCHI KOUHEI;

INT.CL. : H01L 21/56

TITLE : SEALING BOARD OF IC CHIP AND SEALING DEVICE



ABSTRACT : PROBLEM TO BE SOLVED: To obtain the sealing board of an IC chip, the method of sealing and a sealing device with high productivity by providing a sealing material sucking hole through which the sealing material applied around the IC chip mounted on a mounting position is sucked and filling the gap between the IC chip and the sealing board with the sucked sealing material.

SOLUTION: A sealing material applying means 14, which moves in the direction of X, Y and Z relatively to a sealing stage 13, applies sealing material 15 around an IC chip 11 mounted on a sealing board 12. The sealing material sucking means 16 sucks the sealing material 15 applied to the IC chip 11 through a sealing material sucking through hole 12a and sealing material sucking hole 13b, and fills the gap between the IC chip 11 and the sealing board 12 with the sucked sealing material 15 by force. Therefore, the productivity is improved drastically compared with the case before of flowing the sealing material into the gap between the IC chip and the board with the help of the inclination of the sealing board for a long time of 10 minutes.

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開平9－64076
(43)公開日　平成９年(1997)３月７日

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ　21/56			Ｈ０１Ｌ　21/56	Ｅ

審査請求　未請求　請求項の数６　ＯＬ　（全５頁）

(21)出願番号　特願平7－217482

(22)出願日　平成７年(1995)８月25日

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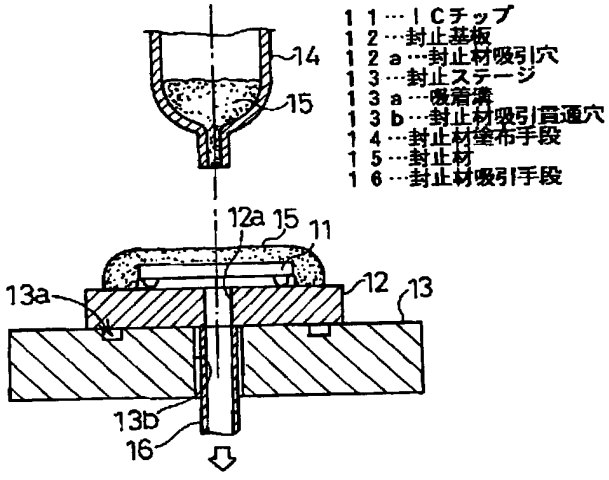
最終頁に続く

(54)【発明の名称】　ＩＣチップの封止基板と封止方法と封止装置

(57)【要約】
【目的】　生産性が高いＩＣチップの封止装置の提供。
【構成】　ＩＣチップ１１をフリップチップ実装する封止基板１２を保持する保持手段１３ａと前記封止基板１２のＩＣチップ実装位置にある封止材吸引穴１２ａに合わせて設けた封止材吸引貫通穴１３ｂとを有する封止ステージ１３と、前記封止基板１２に実装されたＩＣチップ１１の周縁に封止材１５を塗布する封止材塗布手段１４と、前記封止材吸引貫通穴１３ｂと前記封止材吸引穴１２ａとを通して前記ＩＣチップ１１の周縁に塗布された封止材１５を吸引し前記ＩＣチップ１１と前記封止基板１２間の隙間を前記の吸引した封止材１５で充填する封止材吸引手段１６とを備える。



【特許請求の範囲】
【請求項１】　ＩＣチップをフリップチップ実装する封止基板のＩＣチップ実装位置に、前記実装位置に実装したＩＣチップの周縁に塗布した封止材を吸引し前記ＩＣチップと前記封止基板間の隙間を前記の吸引した封止材で充填する封止材吸引穴を設けたことを特徴とするＩＣチップの封止基板。
【請求項２】　ＩＣチップをフリップチップ実装する封止基板のＩＣチップ実装位置に、前記実装位置に実装したＩＣチップを封止する封止材を前記ＩＣチップと前記封止基板間の隙間に注入する封止材注入穴を設けたことを特徴とするＩＣチップの封止基板。
【請求項３】　ＩＣチップをフリップチップ実装する封止基板のＩＣチップ実装位置に封止材吸引穴を設け、前記実装位置にＩＣチップを実装し、前記実装したＩＣチップの周縁に封止材を塗布し、前記ＩＣチップを実装した封止基板面の裏側の前記封止材吸引穴より前記塗布された封止材を吸引し前記ＩＣチップと前記封止基板間の隙間を前記の吸引した封止材で充填することを特徴とするＩＣチップの封止方法。
【請求項４】　ＩＣチップをフリップチップ実装する封止基板のＩＣチップ実装位置に封止材注入穴を設け、前記実装位置にＩＣチップを実装し、前記ＩＣチップを実装した封止基板面の裏側の前記封止材注入穴より封止材を注入し前記ＩＣチップと前記封止基板間の隙間を前記の注入した封止材で充填することを特徴とするＩＣチップの封止方法。
【請求項５】　ＩＣチップをフリップチップ実装する封止基板を保持する保持手段と前記封止基板のＩＣチップ実装位置にある封止材吸引穴に合わせて設けた封止材吸引貫通穴とを有する封止ステージと、前記封止基板に実装されたＩＣチップの周縁に封止材を塗布する封止材塗布手段と、前記封止材吸引貫通穴と前記封止材吸引穴とを通して前記ＩＣチップの周縁に塗布された封止材を吸引し前記ＩＣチップと前記封止基板間の隙間を前記の吸引した封止材で充填する封止材吸引手段とを備えることを特徴とするＩＣチップの封止装置。
【請求項６】　ＩＣチップをフリップチップ実装する封止基板を保持する保持手段と前記封止基板のＩＣチップ実装位置にある封止材注入穴に合わせて設けた封止材注入貫通穴とを有する封止ステージと、前記封止材注入貫通穴と前記封止材注入穴とを通して封止材を注入し前記ＩＣチップと前記封止基板間の隙間を前記の注入した封止材で充填する封止材注入手段とを備えることを特徴とするＩＣチップの封止装置。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、フリップチップ実装工程でのＩＣチップの封止方法とその基板に関するものである。
【０００２】
【従来の技術】最近になって脚光を浴びてきたフリップチップ実装工程やフリップチップ実装を利用したＭＣＭ（マルチチップモジュール）実装工程において、ＩＣチップ実装後に行う封止方法としては、従来から図５に示す方法が一般的である。
【０００３】図５において、封止方法の従来例は、所定温度、例えば６０°Ｃに加熱され、水平面に対し所定角度θ、例えば１５°傾けたブロック１の上に、ＩＣチップ２が実装された基板３を吸着固定し、ディスペンサー４により封止材（エポキシフェノール樹脂）５を、ＩＣチップ２の上辺部２ａに塗布し、封止材５が、１５°の傾斜によってＩＣチップ２と基板３との間に流れ込んで封止するものである。
【０００４】
【発明が解決しようとする課題】しかし、上記の従来例の構成では、傾斜による封止材の流れで封止を行うので封止時間が長く１個のＩＣチップの封止に約１０分かかり生産性が低いという問題点がある。生産量を多くするには、封止作業をするステージ数を多くする必要があり、設備コストが高くなるという問題点につながる。
【０００５】本発明は、上記の問題点を解決し、生産性が高いＩＣチップの封止基板と封止方法と封止装置の提供を目的とする。
【０００６】
【課題を解決するための手段】本願第１発明のＩＣチップの封止基板は、上記の課題を解決するために、ＩＣチップをフリップチップ実装する封止基板のＩＣチップ実装位置に、前記実装位置に実装したＩＣチップの周縁に塗布した封止材を吸引し前記ＩＣチップと前記封止基板間の隙間を前記の吸引した封止材で充填する封止材吸引穴を設けたことを特徴とする。
【０００７】本願第２発明のＩＣチップの封止基板は、上記の課題を解決するために、ＩＣチップをフリップチップ実装する封止基板のＩＣチップ実装位置に、前記実装位置に実装したＩＣチップを封止する封止材を前記ＩＣチップと前記封止基板間の隙間に注入する封止材注入穴を設けたことを特徴とする。
【０００８】本願第３発明のＩＣチップの封止方法は、上記の課題を解決するために、ＩＣチップをフリップチップ実装する封止基板のＩＣチップ実装位置に封止材吸引穴を設け、前記実装位置にＩＣチップを実装し、前記実装したＩＣチップの周縁に封止材を塗布し、前記ＩＣチップを実装した封止基板面の裏側の前記封止材吸引穴より前記塗布された封止材を吸引し前記ＩＣチップと前記封止基板間の隙間を前記の吸引した封止材で充填することを特徴とする。
【０００９】本願第４発明のＩＣチップの封止方法は、上記の課題を解決するために、ＩＣチップをフリップチップ実装する封止基板のＩＣチップ実装位置に封止材注

入穴を設け、前記実装位置にＩＣチップを実装し、前記ＩＣチップを実装した封止基板面の裏側の前記封止材注入穴より封止材を注入し前記ＩＣチップと前記封止基板間の隙間を前記の注入した封止材で充填することを特徴とする。

【００１０】本願第５発明のＩＣチップの封止装置は、上記の課題を解決するために、ＩＣチップをフリップチップ実装する封止基板を保持する保持手段と前記封止基板のＩＣチップ実装位置にある封止材吸引穴に合わせて設けた封止材吸引貫通穴とを有する封止ステージと、前記封止基板に実装されたＩＣチップの周縁に封止材を塗布する封止材塗布手段と、前記封止材吸引貫通穴と前記封止材吸引穴とを通して前記ＩＣチップの周縁に塗布された封止材を吸引し前記ＩＣチップと前記封止基板間の隙間を前記の吸引した封止材で充填する封止材吸引手段とを備えることを特徴とする。

【００１１】本願第６発明のＩＣチップの封止装置は、上記の課題を解決するために、ＩＣチップをフリップチップ実装する封止基板を保持する保持手段と前記封止基板のＩＣチップ実装位置にある封止材注入穴に合わせて設けた封止材注入貫通穴とを有する封止ステージと、前記封止材注入貫通穴と前記封止材注入穴とを通して封止材を注入し前記ＩＣチップと前記封止基板間の隙間を前記の注入した封止材で充填する封止材注入手段とを備えることを特徴とする。

【００１２】

【作用】本願第１発明のＩＣチップの封止基板と、本願第３発明のＩＣチップの封止方法と、本願第５発明のＩＣチップの封止装置とは、封止基板が、ＩＣチップをフリップチップ実装すべき位置に封止材吸引穴を有し、封止ステージが、前記封止基板を保持する保持手段と前記封止基板のＩＣチップ実装位置にある封止材吸引穴に合わせて設けた封止材吸引貫通穴とを有し、封止材塗布手段が、前記封止基板に実装されたＩＣチップの周縁に封止材を塗布し、封止材吸引手段が、前記封止材吸引貫通穴と前記封止材吸引穴とを通して前記ＩＣチップの周縁に塗布された封止材を吸引し前記ＩＣチップと前記封止基板間の隙間を前記の吸引した封止材で強制的に充填するので、従来例では、封止基板の傾斜を利用し、１０分位の長い時間をかけて封止材をＩＣチップと封止基板間の隙間に流し込むのに比較して、生産性が大幅に向上する。

【００１３】本願第２発明のＩＣチップの封止基板と、本願第４発明のＩＣチップの封止方法と、本願第６発明のＩＣチップの封止装置とは、封止基板が、ＩＣチップをフリップチップ実装すべき位置に封止材注入穴を有し、封止ステージが、前記封止基板を保持する保持手段と前記封止基板のＩＣチップ実装位置にある封止材注入穴に合わせて設けた封止材注入貫通穴とを有し、封止材注入手段が、前記封止材注入貫通穴と前記封止材注入穴とを通して封止材を注入し前記ＩＣチップと前記封止基板間の隙間を前記封止材で強制的に充填するので、従来例では、封止基板の傾斜を利用し、１０分位の長い時間をかけて封止材をＩＣチップと基板間の隙間に流し込むのに比較して、生産性が大幅に向上する。

【００１４】

【実施例】本発明のＩＣチップの封止基板とＩＣチップの封止方法とを使用するＩＣチップの封止装置の第１実施例を図１、図２に基づいて説明する。

【００１５】図１、図２において、ＩＣチップ１１が封止基板１２にフリップチップ実装されている。封止基板１２が、ＩＣチップ１１をフリップチップ実装すべき位置に封止材吸引穴１２ａを有し、封止ステージ１３が、ＩＣチップをフリップチップ実装すべき基板を吸着して保持する吸着溝１３ａと封止基板１２のＩＣチップ実装位置にある封止材吸引穴１２ａに合わせて設けた封止材吸引貫通穴１３ｂとを有し、封止ステージ１３に対してＸＹＺ方向に相対移動できる封止材塗布手段１４が、封止基板１２に実装されたＩＣチップ１１の周縁に封止材１５を塗布し、封止材吸引手段１６が、前記封止材吸引貫通穴１２ａと前記封止材吸引穴１３ｂとを通してＩＣチップ１１に塗布された封止材１５を吸引し前記ＩＣチップ１１と前記封止基板１２間の隙間を前記の吸引した封止材１５で強制的に充填するので、従来例では、封止基板の傾斜を利用し、１０分位の長い時間をかけて封止材をＩＣチップと基板間の隙間に流し込むのに比較して、生産性が大幅に向上する。

【００１６】この場合、図２ではＩＣチップ１１全体に封止材１５を塗布しているが、上記のように、ＩＣチップ１１の周縁、即ち、ＩＣチップ１１の各辺に封止材１５を塗布すれば、封止材吸引手段１６の吸引によって、封止材１５を前記ＩＣチップ１１と前記封止基板１２間の隙間に強制的に充填することができる。

【００１７】又、本実施例では、封止基板１２にＩＣチップ１個を実装し封入しているが、１個には限らず、勿論、複数個の場合もある。

【００１８】本発明のＩＣチップの封止基板とＩＣチップの封止方法とを使用するＩＣチップの封止装置の第２実施例を図３、図４に基づいて説明する。

【００１９】図３、図４において、ＩＣチップ２１が封止基板２２にフリップチップ実装されている。そして、ＩＣチップ２１はＩＣ吸着ツール２６によって吸着保持されている。封止基板２２が、ＩＣチップ２１をフリップチップ実装すべき位置に封止材注入穴２２ａを有し、封止ステージ２３が、ＩＣチップ２１をフリップチップ実装すべき封止基板２２を吸着して保持する吸着溝２３ａと前記封止基板２２のＩＣチップ実装位置にある封止材注入穴２２ａに合わせて設けた封止材注入貫通穴２３ｂとを有し、封止材注入手段２４が、前記封止材注入貫通穴２３ｂと前記封止材注入穴２２ａとを通して封止材

２５を注入し前記ＩＣチップ２１と前記封止基板２２間の隙間を前記の注入した封止材２５で強制的に充填するので、従来例では、封止基板の傾斜を利用し、１０分位の長い時間をかけて封止材をＩＣチップと封止基板間の隙間に流し込むのに比較して、生産性が大幅に向上する。

【００２０】この場合、封入材の温度管理による粘度の調整を適正に行えば、フリップチップ実装中に、並行して封止を行うことが可能である。

【００２１】又、図４のＩＣ吸着ツール２６と封止材注入手段２４との上下関係を逆にすれば、重力が注入方向に作用し注入が容易になる。

【００２２】

【発明の効果】本願第１発明のＩＣチップの封止基板と、本願第３発明のＩＣチップの封止方法と、本願第５発明のＩＣチップの封止装置とは、封止材吸引手段が、ＩＣチップの周縁に塗布された封止材を吸引しＩＣチップと封止基板間の隙間を吸引した封止材で強制的に充填するので、従来例では、封止基板の傾斜を利用し、１０分位の長い時間をかけて封止材をＩＣチップと封止基板間の隙間に流し込むのに比較して、生産性が大幅に向上するという効果を奏する。

【００２３】本願第２発明のＩＣチップの封止基板と、本願第４発明のＩＣチップの封止方法と、本願第６発明のＩＣチップの封止装置とは、封止材注入手段が、封止材を注入しＩＣチップと封止基板間の隙間を注入した封止材で強制的に充填するので、従来例では、封止基板の傾斜を利用し、１０分位の長い時間をかけて封止材をＩＣチップと封止基板間の隙間に流し込むのに比較して、生産性が大幅に向上するという効果を奏する。

【図面の簡単な説明】

【図１】本発明のＩＣチップの封止基板とＩＣチップの封止方法とを使用するＩＣチップの封止装置の第１実施例の斜視図である。

【図２】本発明のＩＣチップの封止基板とＩＣチップの封止方法とを使用するＩＣチップの封止装置の第１実施例の断面図である。

【図３】本発明のＩＣチップの封止基板とＩＣチップの封止方法とを使用するＩＣチップの封止装置の第２実施例の斜視図である。

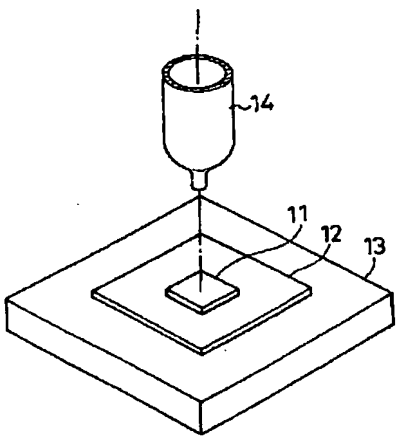
【図４】本発明のＩＣチップの封止基板とＩＣチップの封止方法とを使用するＩＣチップの封止装置の第２実施例の断面図である。

【図５】従来例のＩＣチップの封止基板とＩＣチップの封止方法とを使用するＩＣチップの封止装置の斜視図である。

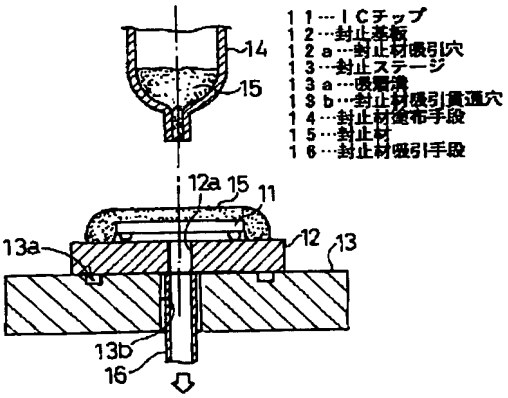
【符号の説明】

１１　ＩＣチップ
１２　封止基板
１２ａ　封止材吸引穴
１３　封止ステージ
１３ａ　吸着溝
１３ｂ　封止材吸引貫通穴
１４　封止材塗布手段
１５　封止材
１６　封止材吸引手段
２１　ＩＣチップ
２２　封止基板
２２ａ　封止材注入穴
２３　封止ステージ
２３ａ　吸着溝
２３ｂ　封止材注入貫通穴
２４　封止材注入手段
１５　封止材
１６　ＩＣ吸着ツール

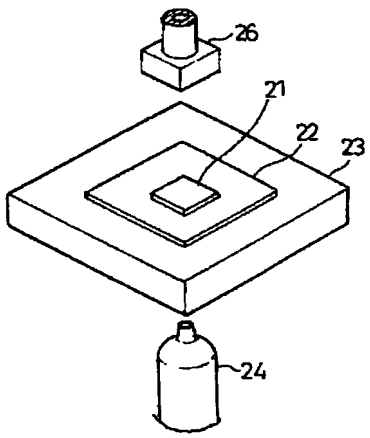
【図１】



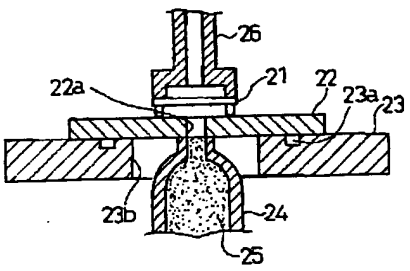
【図２】



【図３】

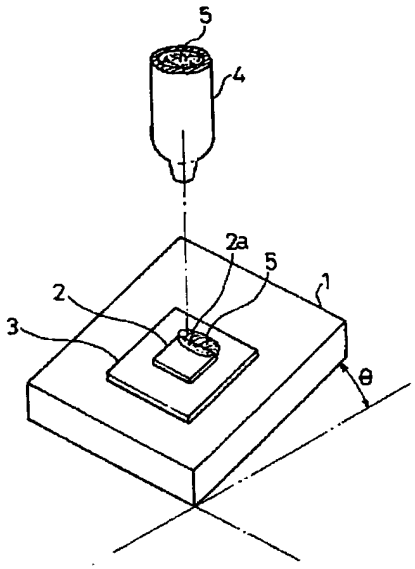


【図4】



21…ICチップ　23b…封止材注入貫通穴
22…封止基板　24…封止材注入手段
22a…封止材注入穴　25…封止材
23…封止ステージ　26…IC吸着ツール
23a…吸着溝

【図5】



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